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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 4 :		(11) International Publication Number: WO 87/ 05429
G09G 3/36	A1	(43) International Publication Date: 11 September 1987 (11.09.87)

(21) International Application Number: PCT/US87/00474

(22) International Filing Date: 10 March 1987 (10.03.87)

(31) Priority Application Number: 838,219

(32) Priority Date: 10 March 1986 (10.03.86)

(33) Priority Country: US

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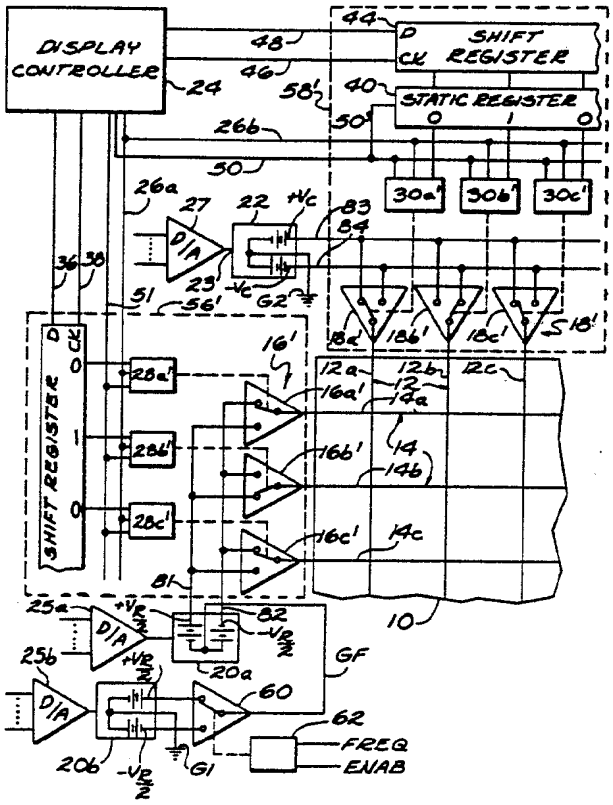
(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), FR (European patent), GB (European patent), IT (European patent), JP, LU (European patent), NL (European patent), SE (European patent).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: LIQUID CRYSTAL DISPLAY HAVING IMPROVED ELECTRODE DRIVE CIRCUITRY

(57) Abstract

A switching circuit (60) for reducing the voltages which must be supported by the driver circuits (16, 18) of a liquid crystal display (10) of the type having row and column electrodes that are driven by squarewave AC drive voltages. The switching circuit is connected to the inputs of the row and/or column driver circuits, the display ground (G1) and the DC source (20a, 20b) from which the squarewave AC drive voltages are derived. The switching circuit is switched in synchronism with the driver circuits and so controls the connections between the display ground, the DC source and the inputs (B1, B2) of the driver circuits that the voltages between those inputs remain less than or equal to the peak value (Vr) of the drive voltages applied to the associated electrodes.



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LIQUID CRYSTAL DISPLAY HAVING IMPROVED ELECTRODE DRIVE CIRCUITRY

Field of the Invention

The present invention relates to matrix type liquid crystal displays and is directed more particularly to a squarewave driven liquid crystal display which includes switching circuitry for reducing the voltages that must be supported by the transistors of the row and/or column driver circuits.

Background of the Invention

In matrix type displays which utilize liquid crystal materials such as the smectic A liquid crystal materials described in U.K. patent application serial number 8518682, filed on July 24, 1985, it has been discovered that the optical state of each picture element of pixel may be controlled solely by controlling the frequencies and amplitudes of the voltages (preferably squarewave AC voltages) which are applied to the row and column electrodes. A pixel may, for example, be rendered opaque or "scattered" by applying between the transparent row and column electrodes which define its position one or more cycles or a squarewave voltage having a relatively low frequency such as 25 Hz and a relatively high amplitude such as 270 volts peak (540 volts peak to peak). After being "scattered" the same pixel may be rendered transparent

of "cleared" by applying between the same row and column electrodes several cycles of a squarewave voltage having a relatively high frequency such as 1500 Hz and a relatively low amplitude such as 175 volts peaks. The pixel may then be returned to its original "scattered" state by re-applying the just mentioned scattering voltages, the transition between the scattered and cleared states being fully reversible by purely electrical means.

In order to reduce the number of physical connections between the row and column electrodes and the external circuitry which determines the image to be displayed, the circuits which drive the row and column electrodes are fabricated in the form of integrated circuits (IC's) that are preferably although not necessarily mounted on and along the edges of the display screen. With this construction the row and column driver circuits generate the voltage necessary to drive respective electrodes upon being supplied with operating voltages and control signals over a relatively small number of leads. The latter number is small because the operating voltage levels and most of the control signals used by the driver circuits are the same for all driver circuits (of a given type) and because the remaining or data signals are supplied to the driver circuits via serially loaded shift registers.

The only significant problem with displays of the above described type is that they require that high voltages be present within the row and column driver circuits. The presence of such high voltages is a problem because it requires the use of high voltage rating transistors and/or relatively complex driver circuit designs. These factors, in turn, cause the driver circuits to be relatively expensive, to occupy relatively large areas within their respective integrated circuits and to operate at relatively high temperatures.

The use of high voltages can also cause the reliability of the display to suffer unless extreme care is taken to assure that all of high voltage transistors of all of the driver circuits meet their full voltage rating and operating temperature specifications.

Summary of the Invention

In accordance with the present invention the above described problem is solved by providing a switching circuit which substantially reduces the voltages which must be supported by the transistors of the row and/or column driver circuits without reducing the drive voltages that are applied to the associated electrodes.

Generally speaking, the switching circuit of the invention comprises circuitry for so controlling the connections between the display ground, the DC source which supplies drive power to the electrodes and the inputs are prevented from rising above the peak values of the drive voltages that are applied to the associated electrodes. In doing so, the switching circuit of the invention causes the electrodes to receive their full rated driving voltages while at the same time eliminating the connections that had in the past caused the inputs of the driver circuits to be exposed to the peak-to-peak values of the drive voltages that were applied to the associated electrodes. As a result, the circuit of the invention allows the driver circuits to be fabricated with lower voltage rating transistors and to use circuit designs having fewer transistors. This, in turn, reduces the size, cost and power dissipated by the driver circuits while at the same time improving their reliability.

In all preferred embodiments, the switching circuit of the invention is a two or more state switching network which is mounted off of the glass panels of the display screen and which has an output or outputs which are

connected to the DC inputs of all of the row driver circuits. This switching circuit is switched in synchronism with the switching of the driver circuits, thereby assuring that its beneficial effect is produced during both half cycles of the desired squarewave electrode drive voltages and during both the scattering and clearing modes of the display. The magnitudes of the DC voltages which are applied to the row driver circuits through the switching circuit of the invention are preferably controlled by the display controller (usually the CPU of the terminal of which the display forms a part) thereby assuring that the electrodes are driven with voltages having magnitudes that are appropriate for both the scattering and clearing modes of the display.

In a first preferred embodiment, the switching circuit of the invention is connected in series with the two parts of the DC source which supplies operating power to the row drivers. In this embodiment the switching circuit maintains a series aiding relationship between the two parts of the DC source for the active (or then connected) input of the selected row driver, with the then required polarity, while at the same time maintaining a series opposing relationship between the two parts of the DC source for the active inputs of all non-selected row drivers. In both cases, however, the switching circuit limits the voltages across the inputs of all of the row drivers to a value approximately equal to the peak value of the drive voltage applied to the selected electrode. As a result, this embodiment of the invention may be characterized as a switchable biasing arrangement or bias driver which maintains the required peak voltage at the output of the selected row driver while limiting the voltages across the inputs of all row drivers to a value approximately equal to that voltage.

In a second preferred embodiment, the switching circuit of the invention is connected across the single DC source which supplies operating power to the row drivers, the voltage across that DC source preferably being equal to that across one of the two parts of the DC source of the first embodiment. In the second embodiment the switching circuit connects the DC source in series with the active input of the selected row driver, with the then required polarity, while at the same time connecting the display ground to the active inputs of all of the non-selected row drivers. Again, however, the switching circuit limits the voltages across the inputs of all of the row drivers to a value approximately equal to the peak value of the drive voltage that is applied to the selected electrode. As a result, this embodiment of the invention may be visualized as a part of a bus switching arrangement or bus driver which maintains the required peak voltage at the output of the selected row driver while limiting the voltages across the inputs of all row drivers to a maximum value equal to that voltage.

Although the switching circuit of the invention is preferably applied only to the row driver circuits, it may also be applied only to the column driver circuits. In addition, the circuit of the invention may be applied both to the row driver circuits and to the column driver circuits. It will therefore be seen that the present invention is applicable to matrix type displays having a variety of different driver circuit configurations.

Brief Description of the Drawings

The above mentioned embodiments and operating principles will be more clearly understood from the following description and drawings in which:

FIG. 1 is a block-schematic diagram of a section of the driver circuitry of a matrix display which does not include the circuitry of the present invention;

FIG. 2 is a block-schematic diagram of a section of the driver circuitry of a matrix display which includes a first embodiment of the switching circuitry of the invention;

FIG. 3 is a block-schematic diagram of a section of the driver circuitry of a matrix display which includes a second embodiment the switching circuitry of the invention;

FIG. 4 is a block-schematic diagram of a section of the driver circuitry of a matrix display in which the switching circuitry of the invention is applied to both the row and column driver circuits;

FIG. 5 is a fragmentary block-schematic diagram of the driver circuitry of a matrix display which includes a third embodiment of the switching circuitry of the invention;

FIG. 6 is a schematic diagram of one type of row or column driver which is suitable for use with the invention;

FIG. 7 is a schematic diagram of one type of switching circuit which is suitable for use in the embodiment of FIG.2;

FIG. 8 is a schematic diagram of one type of switching circuit which is suitable for use in the embodiments of FIGS. 3 and 4; and

FIG. 9 is a schematic diagram of one type of switching circuit which is suitable for use in the embodiment of FIG.5.

Detailed Description

Referring to FIG. 1 there is shown a block-schematic diagram of a portion of a matrix type liquid crystal display which does not include the switching circuitry of the present invention. This display includes a display screen 10 (of which only the upper left corner is shown) that includes two parallel plates of glass which are separated by a thin layer of a suitable liquid crystal material, such as that disclosed in the above referenced U.K. patent applications. The inner surfaces of these plates support an array of transparent column electrodes 12 and an orthogonally oriented array of transparent row electrodes 14, individual electrodes of each type being distinguished by the postscripts a, b, c, etc. The volumes of liquid crystal material which are located in the spaces between the intersections of these row and column electrodes comprise the picture elements or pixels which form the image to be displayed on screen 10.

In order to cause any pixel to change from its scattered or opaque state to its cleared or transparent state or vice versa, one or more pulses of squarewave AC voltages having the proper frequency and amplitude are applied to the row and column electrodes that are associated with that pixel. With the above mentioned schematic A liquid crystal material, for example, a pixel is scattered when a single voltage pulse having a frequency of 25 Hz and an amplitude of 270 volts peak is applied thereacross, and is cleared when a series of voltage pulses having a frequency of 1500 Hz and a amplitude of 175 volts peak is applied thereacross. Ordinarily these voltages are applied across a pixel by applying one voltage, known as the row drive voltage, to the respective row electrode and a second voltage, known as the column drive voltage, to the respective column electrode. The difference

between these two voltages, or row-column difference voltage, constitutes the total drive voltage across the pixel.

In the display of FIG. 1 the row drive voltages are applied to the row electrodes by respective ones of row driver circuits 16 and the column drive voltages are applied to the column electrodes by respective ones of column drive circuits 18, the individual driver circuits or drivers being distinguished by the postscripts a, b, c, etc. These drivers typically comprise multi-state solid-state switching networks which generate the desired squarewave AC voltages from a center-tapped DC source having a positive terminal, a negative terminal and a neutral terminal electrically therebetween. Row drivers 16, for example, generate the row drive voltages from a first center-tapped DC source 20 by switchably connecting their outputs either to the positive output terminal of source 20 via a positive bus B1 to establish the positive half cycle of the AC voltage, or to the negative output terminal of source 20 via a negative bus B2 to establish the negative half cycle of the AC voltage, or to the neutral terminal of source 20 which is connected to display ground terminal G1. The latter connection is necessary because the display of FIG. 1 is driven on a row at a time basis, i.e., with an AC row drive voltage being applied to only one row electrode at a time (the selected row) while zero volts is applied to all of the remaining or non-selected rows. In FIG. 1 the selected row is 14b, as is indicated by the off zero position of the switch in row driver 16b, while all other rows are non-selected rows, as is indicated by the on-zero positions of the switches in all other row drivers. Because the internal structure and operation of the row drivers of FIG. 1 form no essential part of the present invention, they will not be described in detail herein.

Similarly, column drivers 18 generate the column drive voltages from a second center-tapped DC source 22 by switchably connecting their outputs to either the positive or negative output terminals of that source. Although the column drivers are usually provided with the ability to establish a zero volt output state (in the interest of their having the same construction as the row drivers), this zero volt output state is not normally used during the operation of the column drivers. This is because display 10 uses a phase control addressing scheme in which column drive voltages are simultaneously applied to all column electrodes, with one phase position being associated with selected columns and a second phase position being associated with non-selected columns.

Assume, for example, that row 14b has been selected and that only the pixel 12b-14b lying at the intersection of that row and column 12b has been selected to undergo a change in state. To produce this change in state column 12b is selected by connecting its drive output to the negative output terminal of DC source 22. This assures that the row and column driver voltages at selected pixel 12b-14b of the selected row have opposite polarities (i.e., are out of phase) and therefore that they combine additively to increase the row-column difference voltage at that pixel. At the same time columns 12a and 12c are non-selected by connecting their driver outputs to the positive terminal of DC source 22. This assures that the row and column drive voltages at non-selected pixels 12a-14b and 12c-14b of the selected row have the same polarity (i.e., are in phase) and therefore that they combine subtractively to decrease the row-column difference voltages at those pixels. Naturally, these states exist for only one half-cycle of the row-column drive voltages; during the other half cycle the states of all switches (except those connected

to display ground G1) are reversed, causing the above described voltage difference relationships to be maintained but with a reversed polarity. Thus, as the drivers switch between their positive and negative states, high magnitude AC drive voltages appear across each selected pixel of the selected row and low magnitude AC drive voltages appear across all non-selected pixels of the selected row. Obviously, the magnitudes of the row and column drive voltages must be chosen so that the high magnitude AC drive voltages are above the threshold voltage of the liquid crystal material for all selected pixels and so that the low magnitude AC drive voltages are below that threshold voltage for all non-selected pixels. In order to assure that the only selected pixels of the selected row will change their optical states.

Because both the amplitudes and frequencies of the voltages associated with the scattering and clearing conditions are different from one another, the transition between these conditions requires both that the magnitudes of the output voltages of DC sources 20 and 22 be changed and that the switching frequencies of all row and column drivers be changed. In FIG. 1 the output voltages of DC sources 20 and 22 are easily changed because both sources comprise power supplies that are programmable, i.e., can be changed by changing the magnitudes of the analog control voltages that are applied to respective control inputs 21 and 23 thereof as, for example, by a display controller 24 via respective digital to analog (D/A) converters 25 and 27. Because such power supplies are well known and are constructed by using integrated circuits sold by Texas Instruments under the designation TL594 in the manner described in Texas Instruments Application Report B-209, they will not be described in detail herein.

In FIG. 1 the switching frequencies of the row and column drivers are easily changed because these frequencies are determined by a frequency control signal FREQ (see FIGS. 2-9) which is generated by display controller 24. The latter signal is applied to the row drivers via conductor 26a and respective row logic networks 28a, 28b, 28c, etc. and to the column drivers via conductor 26b and respective column logic networks 30a, 30b, 30c, etc. The latter networks control the instantaneous states of the driver switches, via the indicated dotted connections, based on the select or data bits which are applied to the inputs thereof by display controller 24. In the case of the row drivers, for example, row logic networks 28a and 28c cause their row drivers to assume their zero volt or non-selected states because they receive 0's from display controller 24 via respective outputs of a row shift register 34. Similarly, row logic network 28b causes its row driver to switch between its positive and negative states at the frequency of the frequency control signal because it receives a 1 from controller 24 via its respective output of shift register 34. In operation display controller 24 selects each row in succession (once during each display frame) by merely shifting the position of the 1 through shift register 34 via data and clock lines 36 and 38.

In the case of the column drivers, on the other hand, column logic networks 30a and 30c cause their column drivers to be non-selected, i.e., to switch between their positive and negative states in phase with the output voltage of selected row driver 16b, because they receive 0's from display controller 24 via respective outputs of a static register 40. Similarly, column logic network 30b causes its column driver to be selected, i.e., to switch between its positive and negative states 180° out of phase with the output voltage of selected

row driver 16b, because it receives a 1 from controller 24 via its respective output of register 40. In operation, display controller 24 successively loads static register 40 with all the 1's and 0's necessary to select or not select each pixel of each complete row of the display. This loading is accompanied by shifting the necessary 1's and 0's into a shift register 44 via clock and data lines 46 and 48 during the time that static register 40 is providing data for the currently selected row, and then simultaneously transferring the data for the next entire row into static register 40 when that next row is selected. The timing of this transfer is controlled by display controller 24 by means of an enable signal ENAB (see FIGS. 2-9) which is applied to static register 40 via an enable line 50. The activity of the column logic networks are coordinated with that of static register 40 by applying the same enable signal in enabling relationship to each of those networks. The activity of the row logic networks are also coordinated with that of static register 40 by applying an enable signal in enabling relationship to each of these networks via an enable line 51. While the latter signal has the same waveform as the enable signal on line 50, it is preferably electrically isolated therefrom as, for example, by opto-electronic coupling devices within controller 24.

Because the internal structure and operation of the row and column logic networks and the display controller of FIG. 1 form no essential part of the present invention, they will not be described in detail herein.

In presenting a complete new image on display screen 10, display controller 24 begins by causing the row and column drivers to scatter all of the pixels of the display. This is accomplished by outputting signals which cause all of these drivers to operate at the scatter frequency and which cause DC sources 20 and 22

to operate at their scatter magnitudes. Thereafter controller displays the image on a row at a time basis by outputting signals which cause the row drivers of each row and the then associated column drivers to operate at the clear frequency (and proper phase) and which cause DC sources 20 and 22 to operate at their clear magnitudes. Because of the storage property of schematic A liquid crystal materials, no row or column driver voltages need be applied to the row or column electrodes of the display in order to maintain an image once that image has been fully presented. When called for by its program, however, display controller 24 may change or update the display by scattering and subsequently selectively clearing of any single row or set of rows of the display.

In order to reduce costs and to achieve the high row and column electrode densities that are necessary to produce a high resolution image, it is desirable although not absolutely essential that the row and column drivers, their associated logic networks, and their associated shift and static registers be fabricated in the form of integrated circuits which are mounted directly on the glass panels of display screen adjacent to the electrodes with which they are associated. Each such integrated circuit will preferably contain all of the driver, logic and register circuitry that is necessary to control a relatively large number (e.g. 20 or more) of the associated electrodes. The boundaries of two such integrated circuits, one associated with the row electrodes and one associated with the column electrodes of FIG. 1, are indicated by the open ended dotted blocks 56 and 58 thereof.

In making the present invention, it was discovered that there is a serious practical problem with circuitry of the above-described type. This problem is that at least some of the transistors within each row and column

driver must be able to support DC voltages equal to the peak-to-peak voltage which that driver applies to the associated electrode. In FIG. 1, for example, the peak output voltage of row driver 16b (i.e., the voltage between display ground G1 and drive output pin 16b-1) is equal to $+V_R$, one-half of the voltage across DC source 20. At the same time, however, the DC voltage between pins 16b-2 and 16b-3 (and between pins 16b-1 and 16b-2) of driver 16b is equal to $+2V_R$. Thus, if the row and column drivers of FIG. 1 are producing a scatter voltage of 270 volts peak, with the row and column drivers each outputting 135 volts peak (270 volts peak-to-peak), each driver must include at least some transistors which have a rating of at least 270 volts.

While current technology permits the fabrication of integrated circuits which include transistors that can support these high voltages, such integrated circuits are relatively costly and complex. In addition, such integrated circuits consume relatively large amounts of power and have a relatively poor reliability. The latter factor is particularly important in large liquid crystal displays since the failure of a single row or column driver transistor will render the associated row or column inoperative and therefore ruin the appearance of the image to be displayed. The significance of this possibility is compounded by the fact that the replacement of one of the integrated circuits such as 56 or 58 of FIG. 1 can be difficult if not impossible.

In accordance with the present invention the above-described problems are eliminated by including in the display circuitry an additional switching circuit for so controlling the connections between the display ground, at least one of the DC sources, and the inputs of the associated drivers that none of the transistors therein must support voltages greater than the peak output

voltages produced by those drivers. This effectively reduces the voltage which must be supported by the high voltage driver transistors by one-half and reduces the power which is dissipated by the associated integrated circuits by approximately one-half. In addition, the switching circuit of the invention allows the drivers to be simplified by reducing from three to two the number of switching states that each driver must be able to assume. Together these effects not only substantially reduce the cost of producing a display, but also increase its reliability.

Referring to FIG. 2 there is shown a display which includes a first preferred embodiment of the invention. This display is similar to that of FIG. 1 in a number of respects, like functioning parts being similarly numbered, and applies to the row and column electrodes patterns of drive voltages which are indistinguishable from those applied to the row and column electrodes of FIG. 1. This display differs from that of FIG. 1, however, in that it includes corresponding but different row and column driver circuits and corresponding but different logic networks, the correspondences and differences being indicated by the addition of a prime to the indicia used in FIG. 1. The display of FIG. 2 also differs from that of FIG. 1 in that it includes an additional switching circuit 60 which is constructed and connected in accordance with one embodiment of the invention. The internal structures of these row and column drivers and of switching circuit 60 will be shown and described later in connection with FIGS. 6-7.

In the embodiment of FIG. 2 DC source 20 of FIG. 1 is replaced by two center-tapped DC sources 20a and 20b or, equivalently, by a two part center-tapped DC source 20a-20b. Each of these sources 20a and 20b may be thought of as including two component DC sources with a

neutral terminal electrically therebetween. In FIG. 2 each of these component sources produces a voltage which is one-half that produced by each of the halves of DC source 20 of FIG. 1. In the case of source 20b this neutral terminal is connected to the display ground G1 and serves as a fixed ground; in the case of source 20a this neutral terminal is connected to the output of switching circuit 60 and serves as a floating ground GF. The voltages produced by DC sources 20a and 20b are controlled by display controller 24, via respective digital analog converters 25a and 25b, in the same manner that DC source 20 was controlled via converter 25 of FIG. 1.

In accordance with an important feature of the present invention, switching circuit 60 of FIG. 2 so controls the connections between display ground G1, DC sources 20a and 20b, and the inputs of the row drivers (via buses B1 and B2) that the maximum voltage that appears between those inputs never exceeds the peak drive voltage V_R that is applied to the selected row electrode. In the embodiment of FIG. 2 this is accomplished by controlling the last mentioned connections so that one of the two component DC sources within source 20a assumes a series aiding relationship with one of the two component DC sources within source 20b with respect to the selected row driver, and yet simultaneously assumes a series opposing relationships with the other of the two component DC sources within source 20b with respect to all of the non-selected row drivers.

Assuming, for example, that only row 14b is to be selected and that the time for producing the positive half-cycle of the row drive voltage has arrived, the switches within switching circuit 60 and those within the row drivers will be in the states shown in FIG. 2. Under this condition it may be shown that switching

circuit 60 causes the path from display ground G1 to selected electrode 14b through the active (then connected) input of driver 16b to include both of the positive ones of the component sources with DC sources 20a and 20b, resulting in a row drive voltage of $+V_R$. At the same time switching circuit 60 causes the path from display ground G1 to non-selected electrodes 14a and 14c through the active inputs of drivers 16a' and 16c' to include the positive one of the component sources within source 20b and the negative one of the component sources within source 20a, resulting in row drive voltages of zero volts. Similar series aiding and series opposing relationships are established between the component sources within sources 20a and 20b and the selected and non-selected rows when the time for the negative half cycle arrives by simply causing the switches of circuit 60 and the row drivers to assume states opposite to those shown in FIG. 2. Thus, the circuit of FIG. 2 produces the same pattern and magnitude of row drive voltages as the circuit of FIG. 1.

In spite of the just described similarity between the electrode drive voltage patterns produced by the circuits of FIGS. 1 and 2, it will be seen that the maximum voltage that must be supported by the transistors of the row drivers of FIG. 2 is equal to the voltage V_R across DC source 20a, i.e., a voltage one-half of that which must be supported by the transistors of the row drivers of FIG. 1. As a result, the integrated circuits of FIG. 2 are less costly, dissipate less heat and are more reliable than those of FIG. 1. In addition, it will be seen that the row drivers of FIG. 2 may have fewer states and therefore may be made less complex than those of FIG. 1, resulting in further cost reductions and further improvements in reliability. Thus, the switching circuit of the invention represents a substantial

improvement in the drive circuitry of liquid crystal displays.

While the full benefit of the present invention is realized by taking advantage of both the above mentioned voltage reduction feature and the above mentioned row driver simplification feature, it is also possible to practice the invention while taking advantage of only the voltage reduction feature. It is possible, for example, in the embodiment of FIG. 2 to use the same three-state row and column drivers and logic networks as were used in FIG. 1. This may be cost effective for instance in a situation in which an existing display of the type shown in FIG. 1 is in effect converted to the type of display shown in FIG. 2 by retrofitting it with switching circuit 60, two part DC source 20a-20b, and the networks such as 62 which control the same.

Referring to FIG. 3 there is shown a display which includes a second embodiment of the invention. The embodiment of FIG. 3 is similar to that of FIG. 2, corresponding parts being similarly numbered, and applies to the row and column electrodes the same pattern of drive voltages as the displays of FIGS. 1 and 2. The embodiment of FIG. 3 differs from that of FIG. 2, however, in that it includes a switching circuit 60' which is configured so as to allow the use of a single non-center-tapped DC power supply 20' to drive the row electrodes. The internal structure of switching circuit 60' will be discussed later in connection with FIG. 8.

As in the case of switching circuit 60 of the embodiment of FIG. 2, switching circuit 60' of the embodiment of FIG. 3 so controls the connections between display ground G1, DC source 20' and the inputs of the row drivers that the maximum voltages between those inputs never exceeds the peak drive voltage V_R that is applied to the selected row electrode. Unlike switching

circuit 60 of FIG. 2, however, switching circuit 60' of FIG. 3 accomplishes this by switchably controlling the connections between display ground G1 and the positive and negative buses B1 and B2 which connect DC source 20' to the inputs of the row drivers.

Assuming for example that only row 14b is to be selected and that the time for producing the positive half cycle of the row voltage has arrived, the switches within switching circuit 60' and those within the row drivers will be in the states shown in FIG. 3. Under this condition it may be shown that switching circuit 60' connects DC source 20' from display ground G1 to selected row 14b through the active (or then connected) input of driver 16b' resulting in a row electrode voltage of $+V_R$. At the same time switching circuit 60' connects display ground G1 to non-selected rows 14a and 14c through the active inputs of drivers 16a' and 16c', resulting in a row electrode voltage of zero volts. Similar conditions are established when the time for the negative half cycle arrives when the switches of circuit 60' and the row drivers are caused to assume states opposite to those shown in FIG. 3. It will therefore be seen that the circuit of FIG. 3 produces the same pattern of row drive voltages as the circuit of FIGS. 1 and 2 while limiting the voltages between the inputs of the row drivers to a maximum of V_R. In addition, since the circuit of FIG. 3 allows the use of two-state row and column drivers, it provides all the benefits of the embodiment of FIG. 2 with even simpler circuitry.

In spite of its greater complexity, there are respects in which the embodiment of FIG. 2 has advantages over the embodiment of FIG. 3. One of these is the greater flexibility which it provides in the choice of the voltages that appear between buses B1 and B2, i.e., between the inputs of the row drivers. With the embodiment

of FIG. 2 it is possible, for example, to cause the output voltage of source 20b to be larger than that of source 20a and thereby cause the maximum voltage between the inputs of the row drivers to be less than the peak voltage that is applied to the selected row electrode. This, in turn, permits so much of the burden of supporting the row-column difference voltage to be shifted to the row drivers that the programmable DC source 22 which supplies the column drivers may be replaced by a fixed or non-programmable DC source. While the adoption of this approach results in the application of non-zero voltages to non-selected row electrodes, such non-zero voltages are harmless provided that they are small enough to prevent the activation of non-selected pixels.

Referring to FIG. 4 there is shown a display which includes still another embodiment of the invention. The display of FIG. 4 is similar to that of FIG. 3 in that it includes a switching circuit 60' which is connected to the row drivers. The display of FIG. 4 differs from that of FIG. 3, however, in two important respects. The first of these is that the embodiment of FIG. 4 also includes a second switching circuit 64 which is similar to switching circuit 60' of FIG. 3 but which is connected to the column drivers. As a result, the embodiment of FIG. 4 serves to limit the voltages across the inputs of both the row and column drivers to values no larger than the peak drive voltages produced by those drivers. Because switching circuits 60' and 64 of FIG. 4 accomplish this limiting action in the manner described in connection with the embodiment of FIG. 3, this aspect of the operation of the embodiment of FIG. 4 will not be described in detail herein.

The second difference between the embodiments of FIG. 3 and 4 is that the latter uses a one-half select addressing scheme while the former uses the previously

described phase control addressing scheme. This means that the magnitudes of the row and column drive voltages V_R and V_C are equal to one another and that non-selected column electrodes are driven with a voltage of zero volts rather than with an AC voltage that is in phase with the drive voltage of the selected row. This one-half select addressing scheme is used in the embodiment of FIG. 4 because it allows column switching circuit 64 to have the same simple structure as row switching circuit 60'. It will be understood, however, that the switching circuit of the invention can also be used in connection with the column drivers without using the one-half select addressing scheme, provided that the column switching circuit has the more complex structure necessary to accommodate the need to simultaneously output two AC voltages having opposite phases. Because the structure of the latter type of switching circuit will be apparent to those skilled in the art, it will not be specifically shown or described herein.

It will also be understood that it is possible to use the switching circuit of the invention in connection with the column drivers without also using such a circuit in connection with the row drivers. Because the configuration of such an embodiment will also be apparent to those skilled in the art, it will also not be specifically shown or described herein.

Referring to FIG. 5 there is shown a fragmentary block-schematic diagram of still another embodiment of the invention. The embodiment of FIG. 5 is structurally similar to that of FIG. 4, like parts being similarly numbered, except that it substitutes a dual mode or three state switching circuit 66 for the single mode or two state switching circuit 64 of FIG. 4. The embodiment of FIG. 5 is operationally different from the embodiment of FIG. 4, however, in that it uses the phase control

addressing scheme described in connection with FIGS. 1-3 rather than the half select addressing scheme described in connection with FIG. 4. Because the row drive IC's of FIGS.4 and 5 are the same, only the circuitry which is associated with column switching 66 has been shown in FIG. 5.

In one of the two operating modes of switching circuit 66 of FIG. 5, established by display controller 24 via a mode control signal MODE during the scattering condition, contact 66-1 (display ground G2) is switched between contact with contacts 66-2 and 66-3 at frequency FREQ and therefore operates in the same manner as switching circuit 64 of FIG. 4. In this mode of operation all of the column drivers switch in phase with one another and thereby apply the desired high magnitude scattering voltages to all of the column electrodes. As this is occurring, switching circuit 66 limits the voltage across the inputs of the column drivers to the peak value of the scattering voltage in the manner described in connection with switching circuit 64 of FIG. 4.

In the other of the two operating modes of switching circuit 66 of FIG. 5, established by controller 24 via mode control signal MODE during the clearing condition, contact 66-6 (display ground G2) makes contact with contact 66-4 (the center tap of DC supply 22') and remains in contact therewith throughout operating in the clearing mode. In this mode of operation the column drive circuitry has the same configuration as the column drive circuitry of FIG. 1 and operates in the manner described in connection with FIG. 1, i.e., without the voltages across the inputs of the column drivers being limited to the peak values of the voltages applied to the column electrodes. This non-limiting mode of operation is acceptable, however, because other voltages which are applied to the column drivers during the clearing condition

are much lower than those applied thereto during the scattering condition. The advantage of this non-limiting mode is that it allows switching circuit 66 to be simpler than would be the case if it had to produce a voltage limiting effect for the column drivers during both the scattering and clearing conditions of the phase control addressing scheme. Examples of circuits which may be used as dual mode switching circuit 66 and as the associated logic network 68 will be described later in connection with FIG. 9.

In view of the foregoing, it will be seen that the switching circuit of the invention may be applied in a variety of different ways. From FIGS. 2 and 3, for example, it is apparent that the invention may be used both in a bias driving configuration with a two part DC source (FIG. 2) and in a non-bias driving or bus driving configuration with a single DC source (FIG.3). From FIGS. 2-5, on the other hand, it is apparent that the invention may be applied to (a) only the row drivers (FIGS. 2 and 3), (b) both the row and column drivers (FIGS. 4 and 5) or (c) only the column drivers. From FIGS. 2-5 it is apparent that the invention may be used both with a one-half select addressing scheme (FIG. 4) and with a phase control addressing scheme (FIGS. 2, 3 and 5). Finally, as will be apparent to those skilled in the art, the switching circuit of the invention may also be applied to discharge type matrix displays, such as those in which pixels are made visible by the breakdown of a gas within a glass envelope which contains a matrix or grid of fine non-transparent wires. It will be understood that all of these variations and their equivalents are within the contemplation of the present invention.

Because the row and column driver circuits, the switching circuits, and logic networks that are associated therewith in FIGS. 2-5 are not of types well known in

the art, representative embodiments thereof will now be shown and briefly described in connection with FIGS. 6-9.

Referring to FIG. 6, there is shown a schematic diagram of a representative one 28b' of the logic networks of FIGS. 2-5 and of a representative one 16b' of one of the row (or column) drivers of FIGS. 2-5. Of these logic network 28b' includes a simple three element circuit which, when enabled, serves to output either an inverted or non-inverted form of frequency control signal FREQ, depending upon the state of the respective output Q(b) of the associated register. In addition, driver 28b' includes two field effect transistors Q1 and Q2 which conduct alternately to produce the two different conductive states shown in the drivers of FIGS. 2-5 and which are controlled by logic network 28b' through intervening transistors Q3-Q6. The latter transistors serve primarily to interface the logic level voltages produced by logic network 28b' and the higher voltages necessary to properly bias and control output transistors Q1 and Q2. Because the operation of the circuit of FIG. 6 will be apparent to those skilled in the art, that operation will not be discussed in detail herein.

Referring to FIG. 7, there is shown a schematic diagram of switching circuit 60 of FIG. 2 and its associated logic network 62. In FIG. 7 network 62 comprises a NAND gate 64 which serves merely to enable or disable the application of frequency control signal FREQ to switching circuit 60. Switching circuit 60 on the other hand includes two field effect transistors Q7 and Q8 which conduct alternately, under control of network 62, to produce the two conductive states described in connection with that circuit in FIG. 2. The conduction of transistors Q7 and Q8 is in turn controlled by transistors Q9 and Q10 which serve to interface them to the logic voltage levels produced by logic network 62. Because the operation

of the circuit of FIG. 7 will be apparent to those skilled in the art, that operation will not be discussed in detail herein.

Referring to FIG. 8, there is shown a schematic diagram of switching circuit 60' of FIGS. 3 and 4 and its associated logic network 62. In FIG. 8 network 62 has the same structure and function as logic network 62 of FIG. 7. Switching circuit 60' includes two field effect transistors Q11 and Q12 which conduct alternately, under the control of network 62, to produce the two conductive states described in connection with that circuit in FIG. 3. The conduction of these transistors is in turn controlled by bipolar interfacing transistors Q13 and Q14. Because the operation of the circuit of FIG. 8 will be apparent to those skilled in the art, that operation will not be discussed in detail herein.

Referring to FIG. 9, there is shown a schematic diagram of switching circuit 66 of FIG. 5 and its associated logic network 68. In the embodiment of FIG. 9 switching circuit 66 includes two switching transistors Q15 and Q16 which conduct alternately at frequency FREQ when controller 24 establishes the scattering condition and drives mode signal MODE to its 1 state. With this alternate conduction circuit 66 acts as a bus switching arrangement similar to switching circuit 64 of FIG. 4 to limit the voltages appearing between the inputs of the column drivers via buses B3 and B4 to the peak value of the scattering voltage applied to the column electrodes. As in the case of transistors Q11 and Q12 of FIG. 8, the conduction of transistors Q15 and Q16 is controlled by frequency control signal FREQ via the gates of logic network 68 and via interfacing transistors Q17 and Q16 when the other control signals applied to the logic network (in this case both ENAB and MODE) are all in their enabling states. When any of these other control

signals is not in its enabling state, transistors Q15 and Q16 both turn off, thereby preventing switching circuit 66 from operating as a bus switching arrangement.

Switching circuit 66 of FIG. 9 also includes two transistors Q19 and Q20 which conduct simultaneously and continuously when controller 24 establishes the clearing condition and drives mode signal MODE to its 0 state. With this continuous conduction (and the accompanying non-conduction of transistors Q15 and Q16) circuit 66 effectively connects the center tap of DC source 22 to display ground G2 and thereby allows the column drivers to be driven in the manner shown and described in connection with FIG. 1, i.e., with no limitation on the voltages across the inputs of the column drivers. The conduction of transistors Q19 and Q20 is controlled by mode control signal MODE via the gates of logic network 68 and via the same interfacing transistors Q17 and Q18 which interface transistors Q15 and Q16. Diodes 72 and 74 serve to prevent display ground G2 from being connected to the center tap of source 22' through either of transistors Q19 and Q20 when these interface transistors are being used in the manner described in connection with operation of switching circuit 66 in the scattering condition. Because the operation of the remaining circuits of FIG. 9 will be apparent to those skilled in the art, the operation of those circuits will not be described in detail herein.

While the circuitry of the invention has been described with reference to a number of specific embodiments, it will be understood that these embodiments are only exemplary and that the true spirit and scope of the present invention should be determined with reference to the appended claims.

WHAT IS CLAIMED IS:

1. In a matrix display having a plurality of row electrodes, a plurality of column electrodes, a display ground and first and second source means for supplying drive power to said electrodes, in combination:

(a) a plurality of first switching means having inputs connected to the first source means for applying AC drive voltages to respective row electrodes;

(b) a plurality of second switching means having inputs connected to the second source means for applying AC drive voltages to respective column electrodes; and

(c) third switching means connected to the display ground, at least one of the source means and the inputs of a plurality of at least one of said first and second switching means, for so controlling the connections between the display ground, said at least one source means and the inputs of said plurality of at least one of said switching means that the voltages across such inputs are less than the peak-to-peak voltages which such switching means apply to their respective electrodes.

2. The display of claim 1 in which the switching of at least one of the switching means to which the third switching means is connected switches approximately 180° out of phase with the switching of the remaining ones of the switching means to which the third switching means is connected.

3. The display of claim 2 in which the switching means which switch in said 180° out of phase condition produce relatively high AC drive voltages while the remaining switching means produce relatively low AC drive voltages.

4. The display of claim 2 in which the switching of those switching means which switch in said 180° out of

phase condition produce relatively high AC drive voltages having a first phase position while the remaining switching means produce relatively high AC drive voltages having a second phase position.

5. The display of claim 1 in which the third switching means includes first and second terminals connected across one of the source means and a third terminal connected to the display ground.

6. The display of claim 1 in which said at least one of the source means includes two DC sources each having a positive terminal, a negative terminal and a neutral terminal, in which the neutral terminal of one of said DC sources is connected to the display ground, and in which the third switching means includes two terminals connected to the positive and negative terminals of said one DC source and the third terminal connected to the neutral terminal of the other DC source.

7. The display of claim 1 in which each of the switching means to which the third switching means is connected has a current rating sufficient to meet the current requirements of the electrode to which it is connected and in which the third switching means has a current rating sufficient to meet the current requirements of all of the electrodes to which such switching means are connected.

8. The display of claim 1 in which the first and second switching means are contained within integrated circuits mounted on the display screen and in which the third switching means is mounted off of the display screen.

9. The display of claim 1 in which at least one of the DC source means is adapted to establish either a first voltage suitable for use in scattering the pixels of the display or a second voltage suitable for use in clearing the pixels of the display.

10. The display of claim 9 in which the switching frequency of all switching means has a first value during the establishment of said first voltage and a second value during the establishment of said second voltage.

11. In a matrix display having a plurality of row electrodes, a plurality of column electrodes, a display ground and first and second source means for supplying drive power to said electrodes, in combination.

(a) a plurality of first switching means having inputs connected to the first source means for applying AC drive voltages to the row electrodes, each of said first switching means having at least two states;

(b) a plurality of second switching means having inputs connected to the second source means for applying AC drive voltages to the column electrodes, each of said second switching means having at least two states; and

(c) third switching means for switchably controlling the connections between the display ground at least one of the source means and the inputs of a plurality of at least one of said first and second switching means, said third switching means having at least two states;

(d) whereby the drive voltages produced by said plurality of said at least one of said switching means depend both on the states of such switching means and on the state of the third switching means.

12. The display of claim 11 in which the switching of at least one of the switching means to which the third switching means is connected is approximately 180° out of phase with the switching of the remaining switching means to which the third switching means is connected.

13. The display of claim 12 in which the switching of the switching means which switches in said 180° out of phase relationship produces a relatively high AC drive voltage and the remaining switching means produce relatively low AC drive voltages.

14. The display of claim 12 in which the switching of those switching means which switch in said 180° out of phase relationship produce relatively high AC drive voltages having a first phase position and the remaining switching means to produce relatively high AC drive voltages having a second phase position.

15. The display of claim 11 in which the third switching means includes first and second terminals connected across one of the source means and a third terminal connected to the display ground.

16. The display of claim 11 in which said at least one of the source means includes two DC sources each having a positive terminal, a negative terminal and a neutral terminal, in which the neutral terminal of one of the DC sources is connected to the display ground, and in which the third switching means includes two input terminals connected to the positive and negative terminals of said one DC source and an output terminal connected to the neutral terminal of the remaining DC source.

17. The display of claim 11 in which each of the switching means to which the third switching means is connected has a current rating sufficient to meet the current requirements of the electrode to which it is connected and in which the third switching means has a current rating sufficient to meet the current requirements of all the electrodes to which such switching means are connected.

18. The display of claim 11 in which the first and second switching means are contained within integrated circuits mounted on the display screen and in which the third switching means is mounted off of the display screen.

19. The display of claim 11 in which at least one of the source means is adapted to establish either a first voltage suitable for use in scattering the pixels of the display or a second voltage suitable for use in clearing the pixels of the display.

20. The display of claim 19 in which the switching frequency of all switching means has a first value during the establishment of said first voltage and a second value during the establishment of said second voltage.

21. In a matrix display having a plurality of row electrodes, a plurality of column electrodes, a display ground and first and second source means for supplying drive power to said electrodes, in combination:

(a) a plurality of first switching means having inputs connected to the first source row means for applying AC drive voltages to the row electrodes;

(b) a plurality of second switching means having inputs connected to the second source means for applying AC drive voltages to the column electrodes;

(c) third switching means for switchably limiting the voltage across the inputs of a plurality of at least one of said first and second switching means to a value less than or equal to the peak value of the AC drive voltages produced by such switching means; and

(d) means for connecting the third switching means to the display ground, to at least one of the source means and to the inputs of said plurality of at least one of said first and second switching means.

22. The display of claims 21 in which one of the source means includes two DC sources each of which includes two component DC sources, and in which the third switching means maintains a series aiding relationship between the component DC sources of said two DC sources for at least one of the first and second switching means while maintaining a series opposing relationship between the component DC sources of said two DC sources for other such switching means of the same type.

23. The display of claim 21 in which one of the source means consists of a single DC source, and in which the third switching means connects said source to one input of each of said plurality of at least one of said first and second switching means while connecting the display ground to another input of each of such switching means.

24. The display of claim 21 in which the first and second switching means are contained within integrated circuits mounted on the display screen and in which the third switching means is mounted off of the display screen.

25. In a matrix display of the type having a plurality of row electrodes, a plurality of column electrodes, a display ground, first DC source means for supplying the

power necessary to drive the row electrodes, and second DC source means for supplying the power necessary to drive the column electrodes, in combination:

(a) a plurality of row drivers, having inputs connected to the first DC source means, for applying AC drive voltages to respective row electrodes;

(b) a plurality of column drivers, having inputs connected to the second DC source means, for applying AC drive voltages to respective column electrodes; and

(c) a switching circuit connected to the display ground, at least one of the DC source means, and a plurality of at least one of said drivers, said switching circuit having:

(i) a first state in which the switching circuit connects said one DC source means to at least one of the electrodes with a first polarity, through a respective driver, while limiting the voltage between the inputs of that driver to a voltage less than the peak to peak drive voltage produced by that driver, and

(ii) a second state in which the switching circuit connects said one DC source means to said at least one of the electrodes with a second polarity, through the respective driver, while limiting the voltage between the inputs of that driver to a value less than said peak to peak voltage.

26. The display of claim 25 in which at least one of said DC source means includes two DC sources each of which includes two component DC sources, in which the component DC sources of one DC source are connected in series across the inputs of said plurality of at least one of said drivers, and in which the switching circuit maintains a component DC source from one DC source in series aiding relationship with a component DC source from the other DC source for at least one electrode.

27. The display of claim 25 in which at least one of said DC source means consists of a single DC source and in which the switching circuit alternately connects the display ground to different inputs of said plurality of at least one of said drivers.

28. The display of claim 25 in which the drivers are contained within integrated circuits mounted on the display screen and in which the switching circuit is mounted off of the display screen.

29. The display of claim 25 in which said voltage less than said peak to peak drive voltage is approximately equal to the peak voltage produced by said driver.

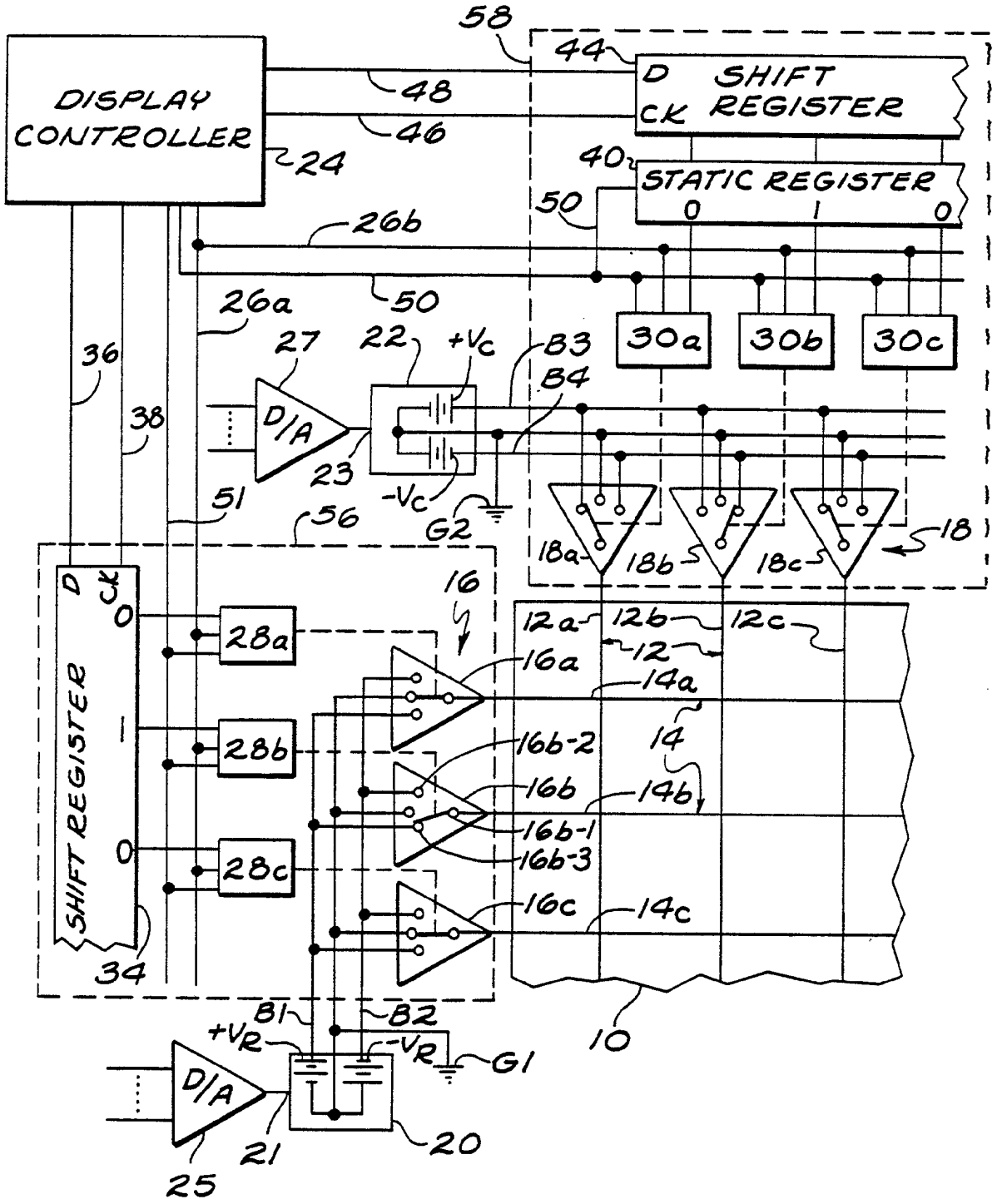
58
44
D SHIFT
CK REGISTER
DISPLAY CONTROLLER
48
46
24
40
STATIC REGISTER
0 1 0
50
26b
26a
50
36
27
22
+Vc
B3
B4
30a
30b
30c
38
D/A
23
-Vc
G2
51
56
18a
18b
18c
18
16
D
CK
0
28a
12a
12b
12c
12
16a
14a
SHIFT REGISTER
28b
16b-2
14
16b
14b
16b-1
16b-3
28c
16c
14c
34
10
B1
B2
+VR
-VR
G1
D/A
21
20
25

FIG. 1

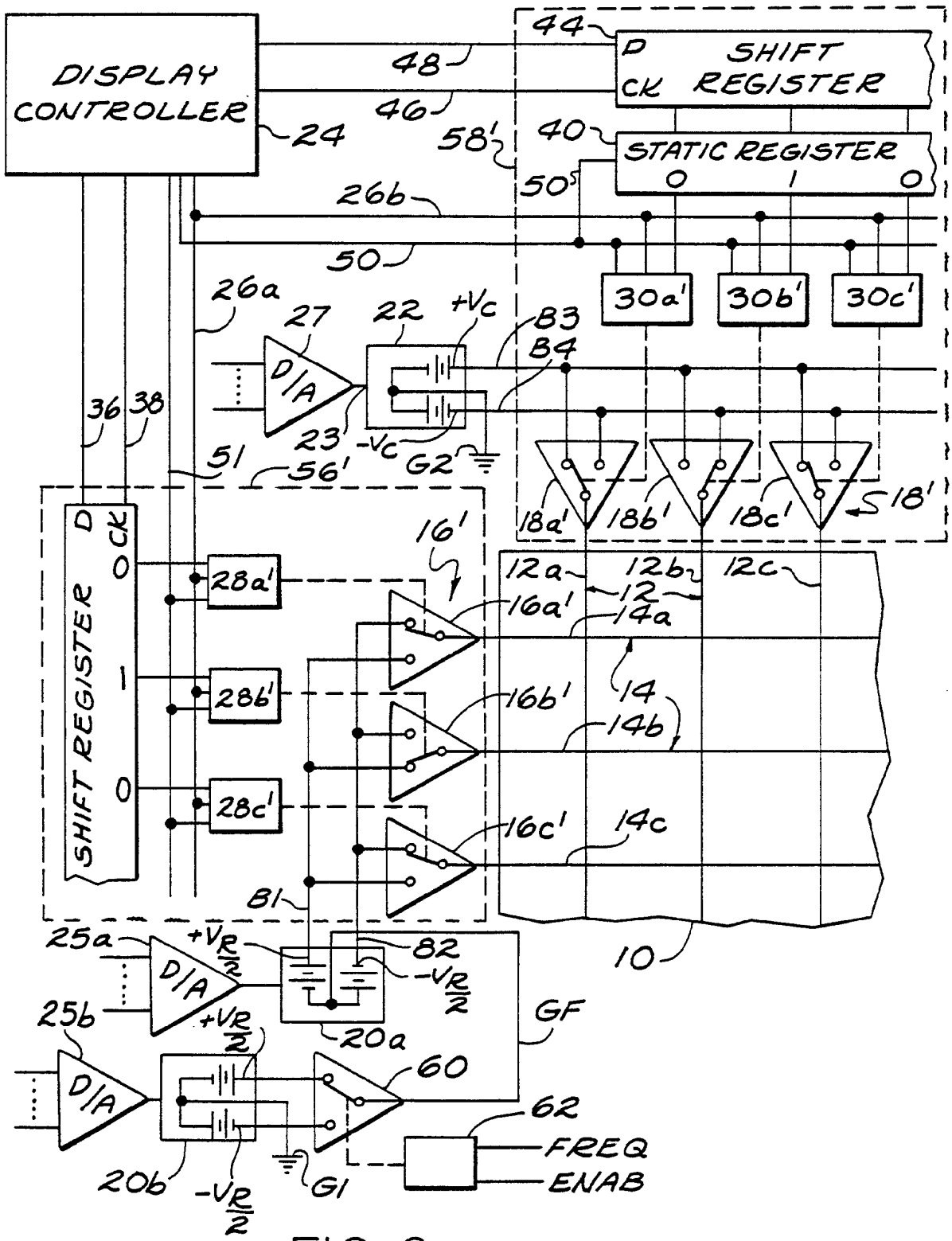
DISPLAY CONTROLLER
24
48
46
44
D
CK
SHIFT REGISTER
40
STATIC REGISTER
0
1
0
58'
50'
50
26b
26a
27
22
+Vc
D/A
23
-Vc
G2
B3
B4
30a'
30b'
30c'
36
38
51
56'
18a'
18b'
18c'
18'
16'
SHIFT REGISTER
D
CK
0
1
0
28a'
28b'
28c'
12a
12b
12c
12
16a'
14a
14
16b'
14b
16c'
14c
B1
10
25a
+VR/2
-VR/2
82
D/A
25b
+VR/2
20a
GF
60
62
FREQ
ENAB
20b
-VR/2
G1

FIG. 2

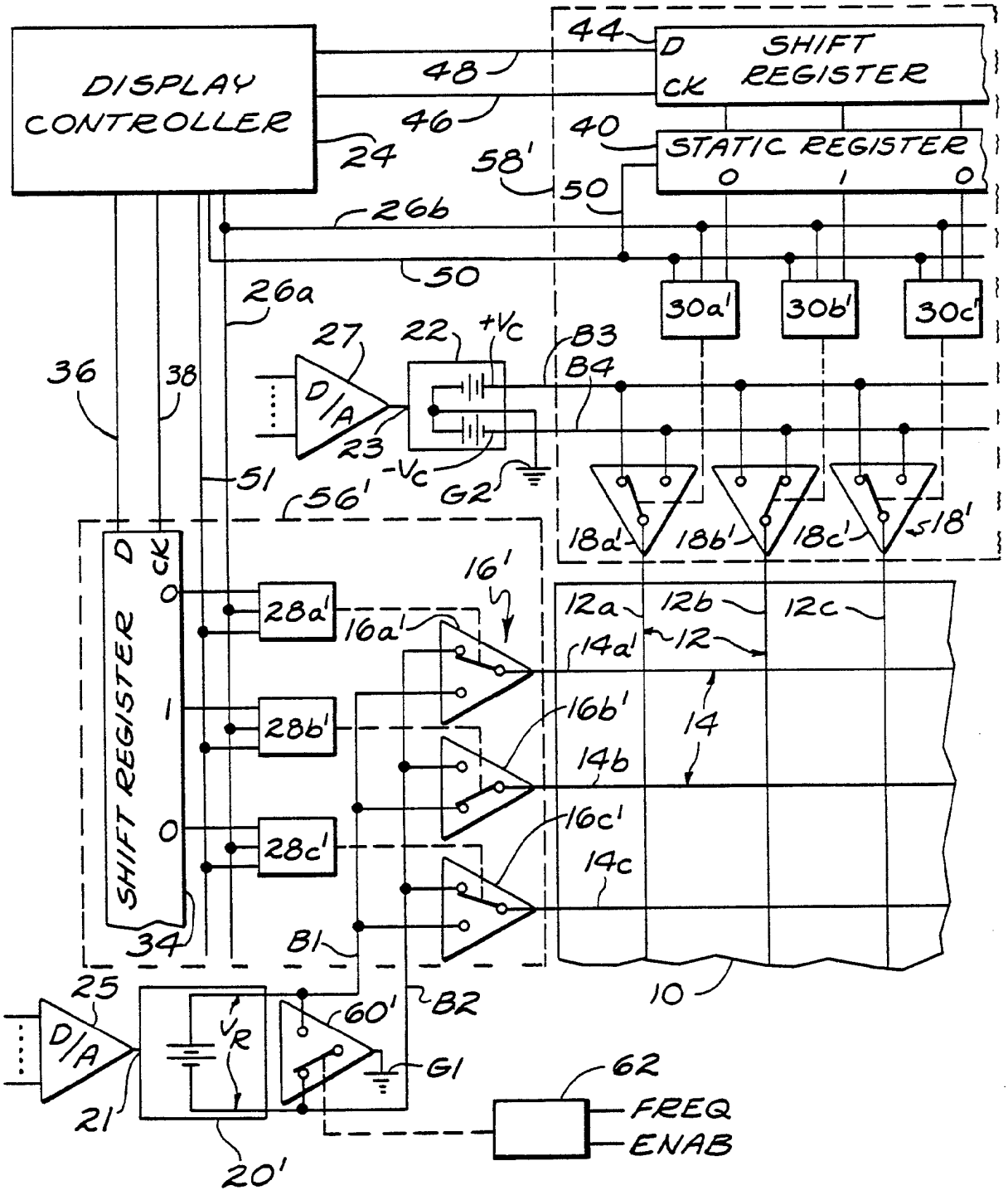
DISPLAY CONTROLLER
48
46
24
44
D
CK
SHIFT REGISTER
40
STATIC REGISTER
0 1 0
58'
50
26b
50
26a
30a'
30b'
30c'
27
22
+Vc
B3
B4
36
38
D/A
23
-Vc
G2
51
56'
18a'
18b'
18c'
18'
16'
SHIFT REGISTER
D
CK
0
1
0
28a'
28b'
28c'
16a'
16b'
16c'
12a
12b
12c
14a'
12
14
14b
14c
34
B1
B2
10
25
D/A
21
VR
60'
G1
62
FREQ
ENAB
20'

FIG. 3

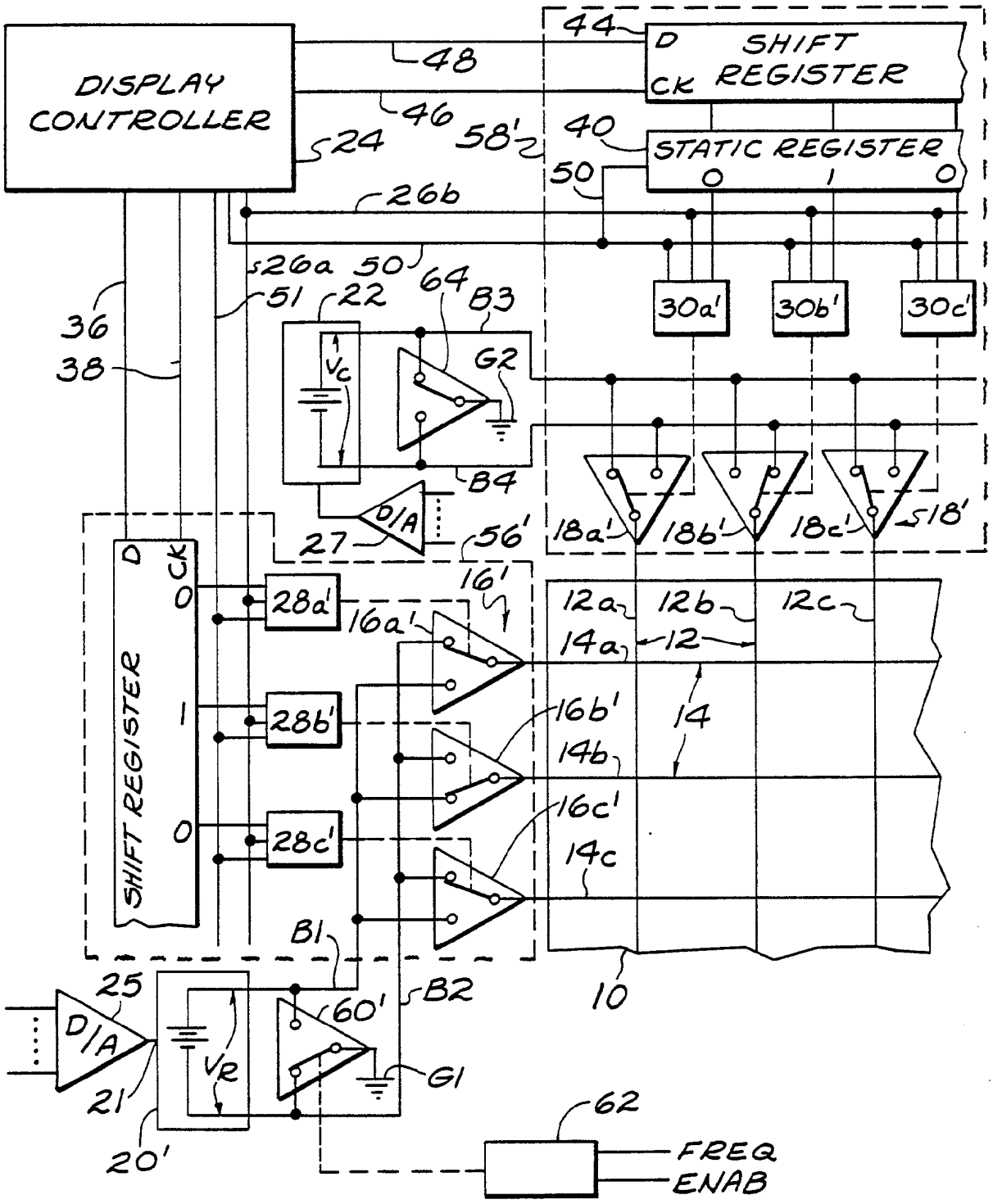
DISPLAY CONTROLLER
48
46
24
58'
44
D
CK
SHIFT REGISTER
40
STATIC REGISTER
0
1
0
50
26b
26a
50
64
B3
51
22
36
38
V_C
G2
30a'
30b'
30c'
B4
D/A
27
56'
18a'
18b'
18c'
18'
16'
D
CK
0
28a'
16a'
12a
12b
12c
14a
12
1
28b'
16b'
14
14b
SHIFT REGISTER
0
28c'
16c'
14c
B1
25
B2
60'
D/A
V_R
G1
21
20'
10
62
FREQ
ENAB

FIG. 4

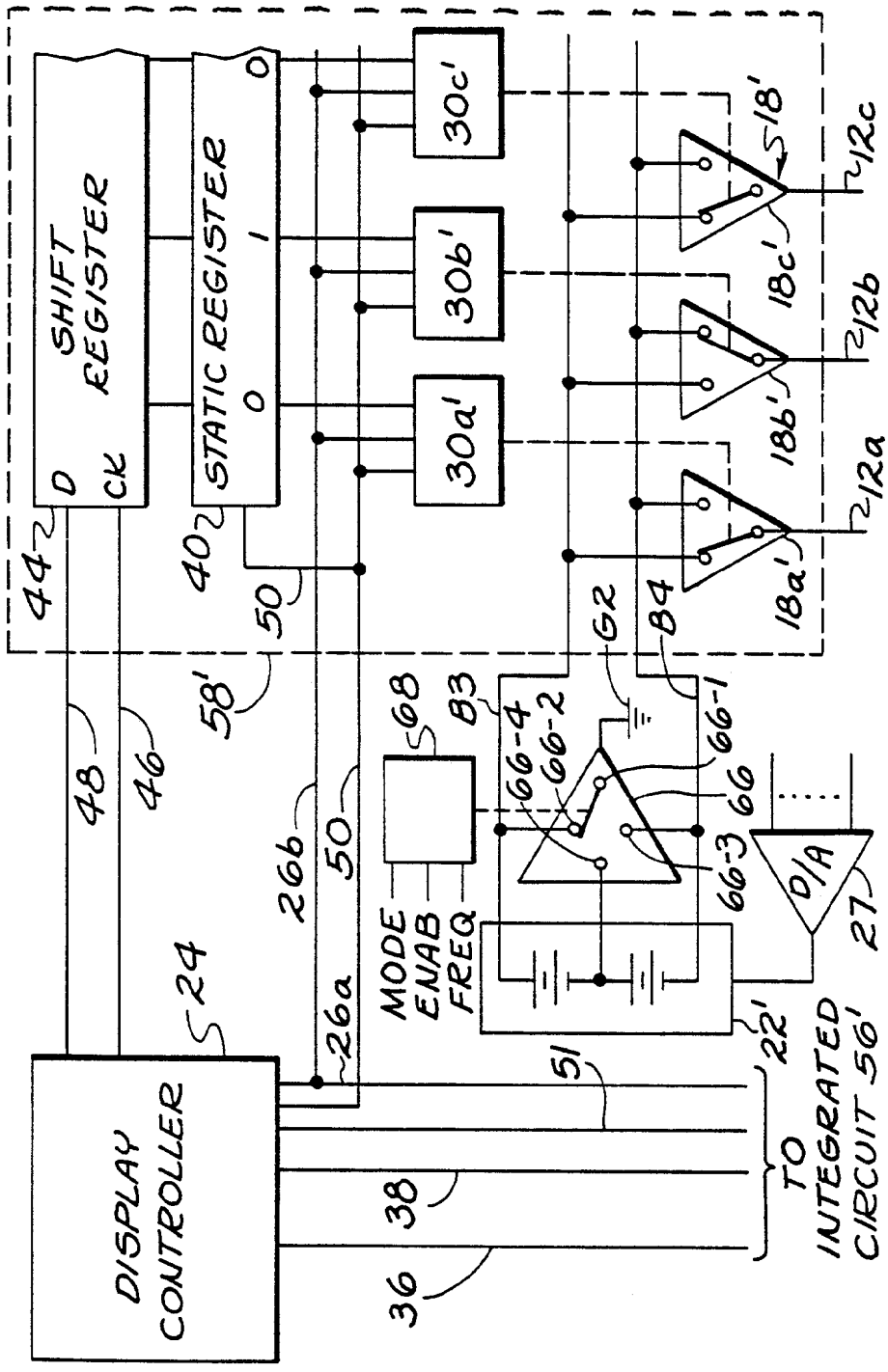
SHIFT REGISTER
D
CK
STATIC REGISTER
0
1
0
44
40
50
58'
30c'
30b'
30a'
18'
18c'
18b'
18a'
12c
12b
12a
62
84
68
83
66-4
66-2
66
66-3
66-1
D/A
27
22'
MODE
ENAB
FREQ
48
46
26b
50
26a
24
51
38
36
DISPLAY CONTROLLER
TO INTEGRATED CIRCUIT 56'

FIG. 5

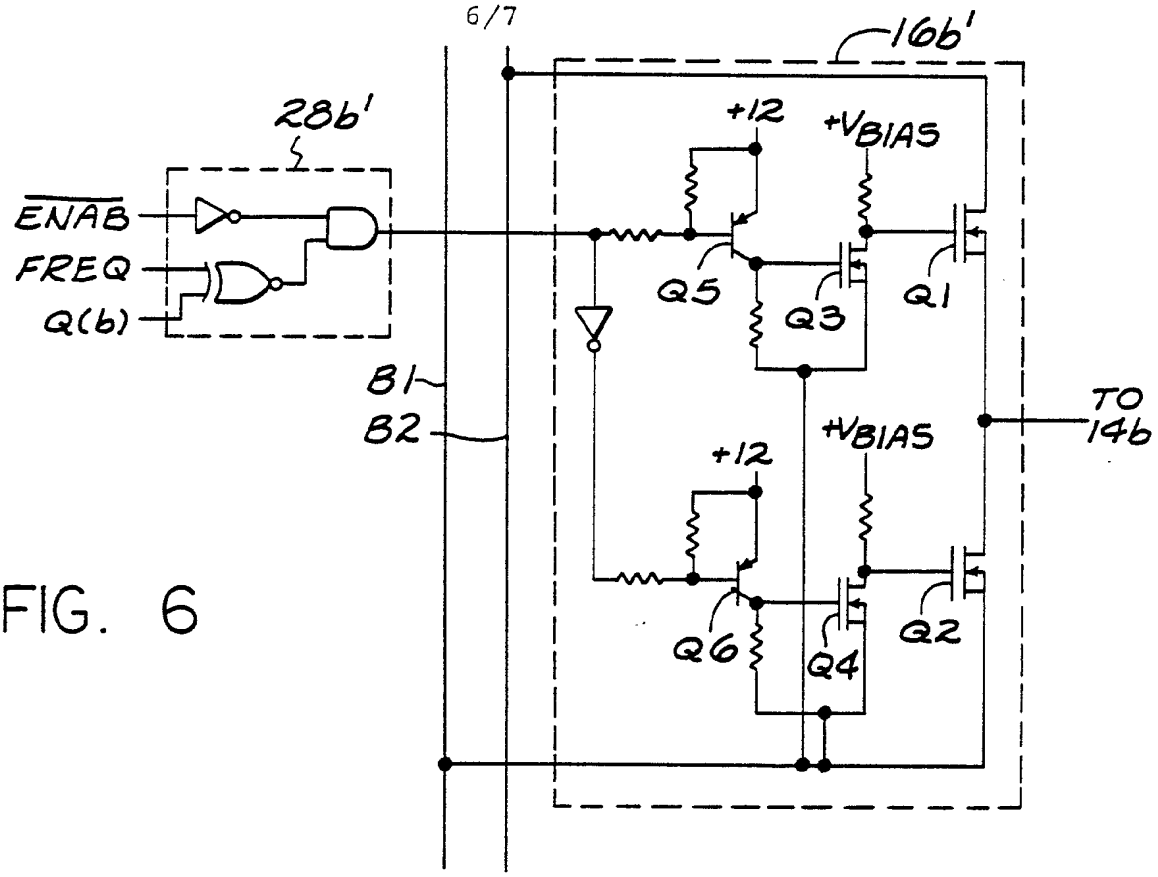
16b'
28b'
+12
+VBIAS
ENAB
FREQ
Q(b)
Q5
Q3
Q1
B1
B2
TO
14b
+VBIAS
+12
Q6
Q4
Q2

FIG. 6

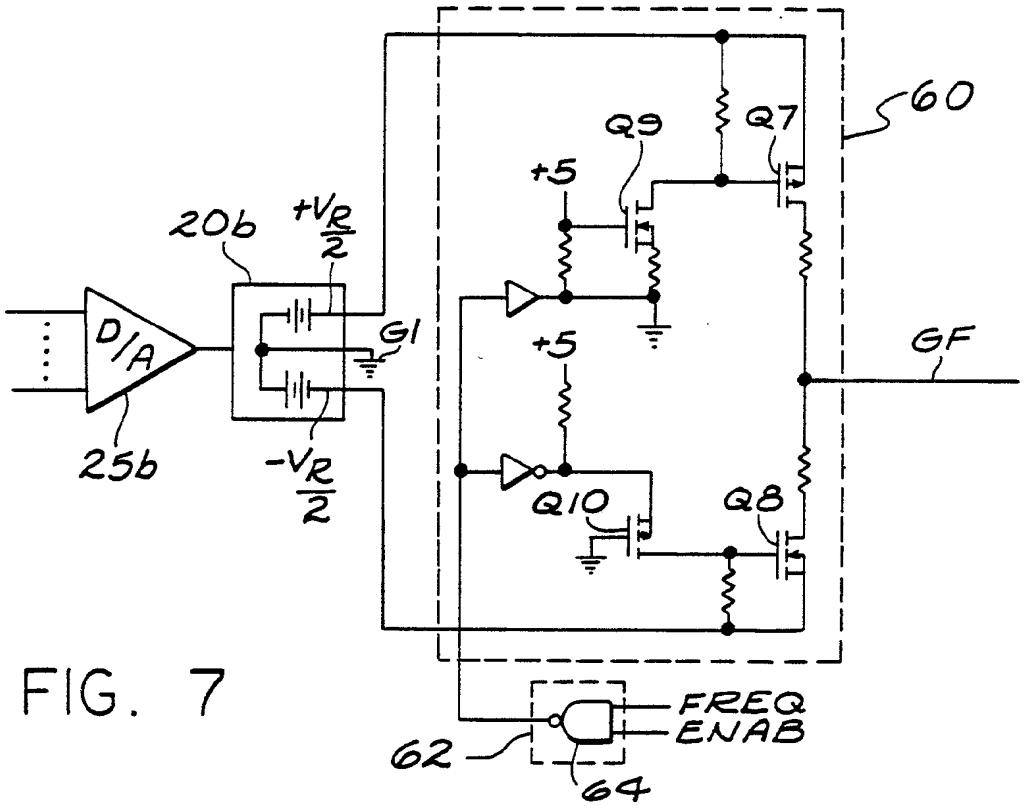
60
Q9
Q7
+5
20b
+VR/2
D/A
G1
GF
+5
25b
-VR/2
Q10
Q8
FREQ
ENAB
62
64

FIG. 7

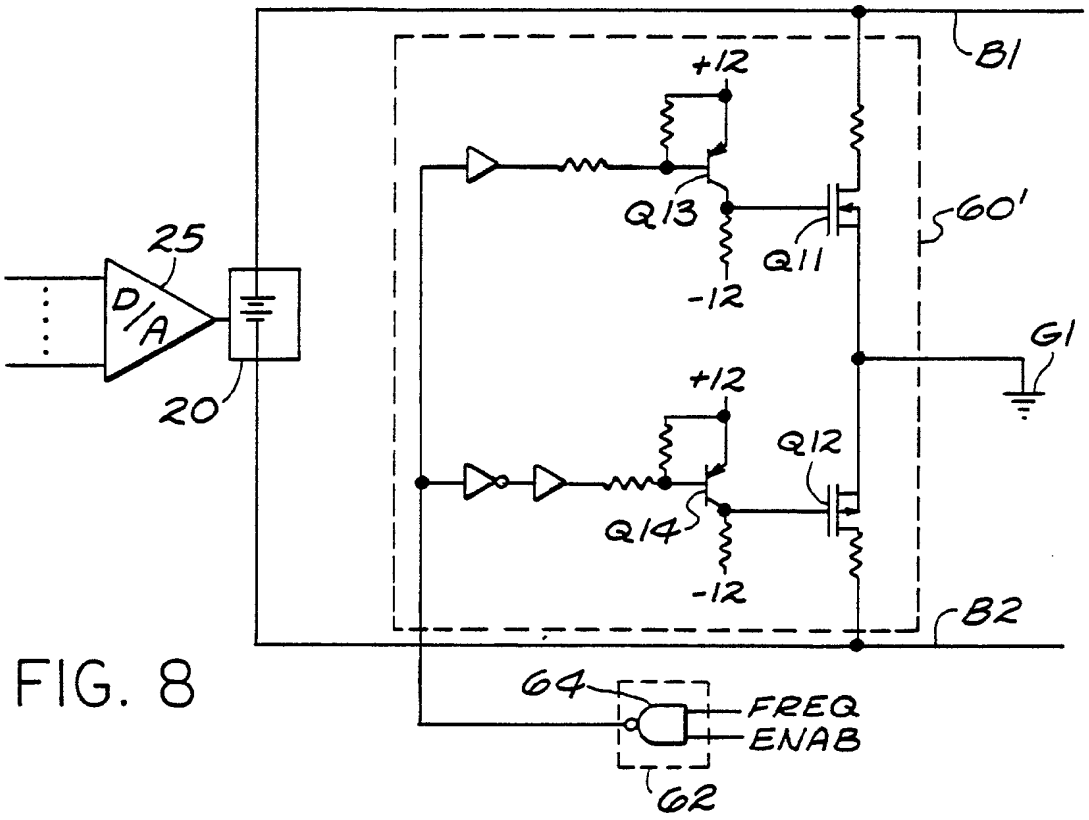
B1
+12
Q13
Q11
60'
-12
25
D/A
20
G1
+12
Q12
Q14
-12
B2
64
FREQ
ENAB
62

FIG. 8

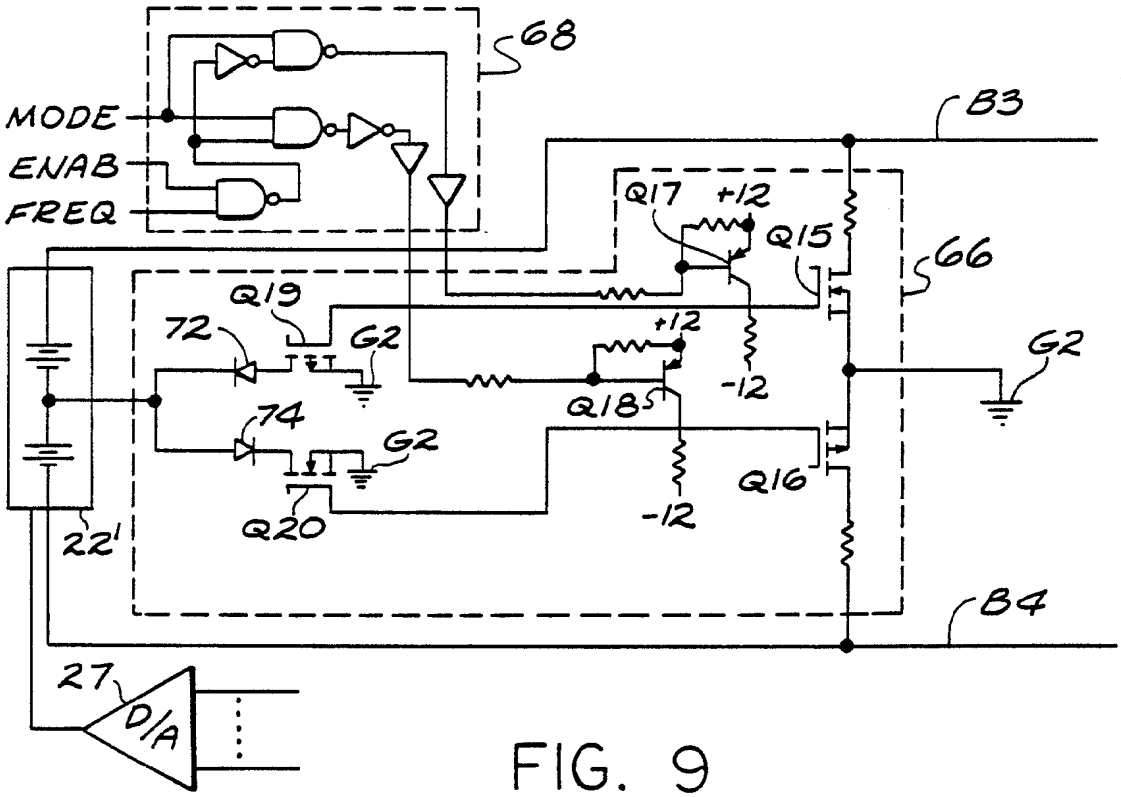
68
MODE
ENAB
FREQ
B3
Q17
+12
Q15
66
Q19
72
G2
+12
G2
Q18
-12
74
G2
Q16
Q20
-12
22'
B4
27
D/A

FIG. 9

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 87/00474

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: G 09 G 3/36

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	G 09 G 3/00

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	DE, A, 2939198 (SIEMENS) 16 April 1981, see page 4, line 32 - page 5, line 26; figure 1	1,11,21
A	--	23,25,27
X	FR, A, 2486694 (NV PHILIPS' GLOEILAMPEN-FABRIEKEN) 15 January 1982, see claims 1,5; figure 3	1,11,21,25
A	-- 1976 SID International Symposium, Digest of Technical Papers, subno. 1, 4-6 May 1976 (Beverly Hills, Los Angeles, USA), C. Suzuki et al., "Character display using thin-film EL panel with inherent memory", see pages 50,51	
A	-- Electronic Applications Bulletin, vol. 35, no. 4, February 1979 (Eindhoven, NL), "Liquid crystal displays-part 2", see pages 172-187	
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* Special categories of cited documents: [10]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
11th June 1987	17 JUL 1987
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	M. VAN MOL

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 87/00474 (SA 16582)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 25/06/87

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Patent document cited in search report	Publication date	Patent family member(s)		Publication date
DE-A- 2939198	16/04/81	None		
FR-A- 2486694	15/01/82	JP-A-	57048785	20/03/82
		DE-A-	3124431	11/03/82
		NL-A-	8003930	01/02/82
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